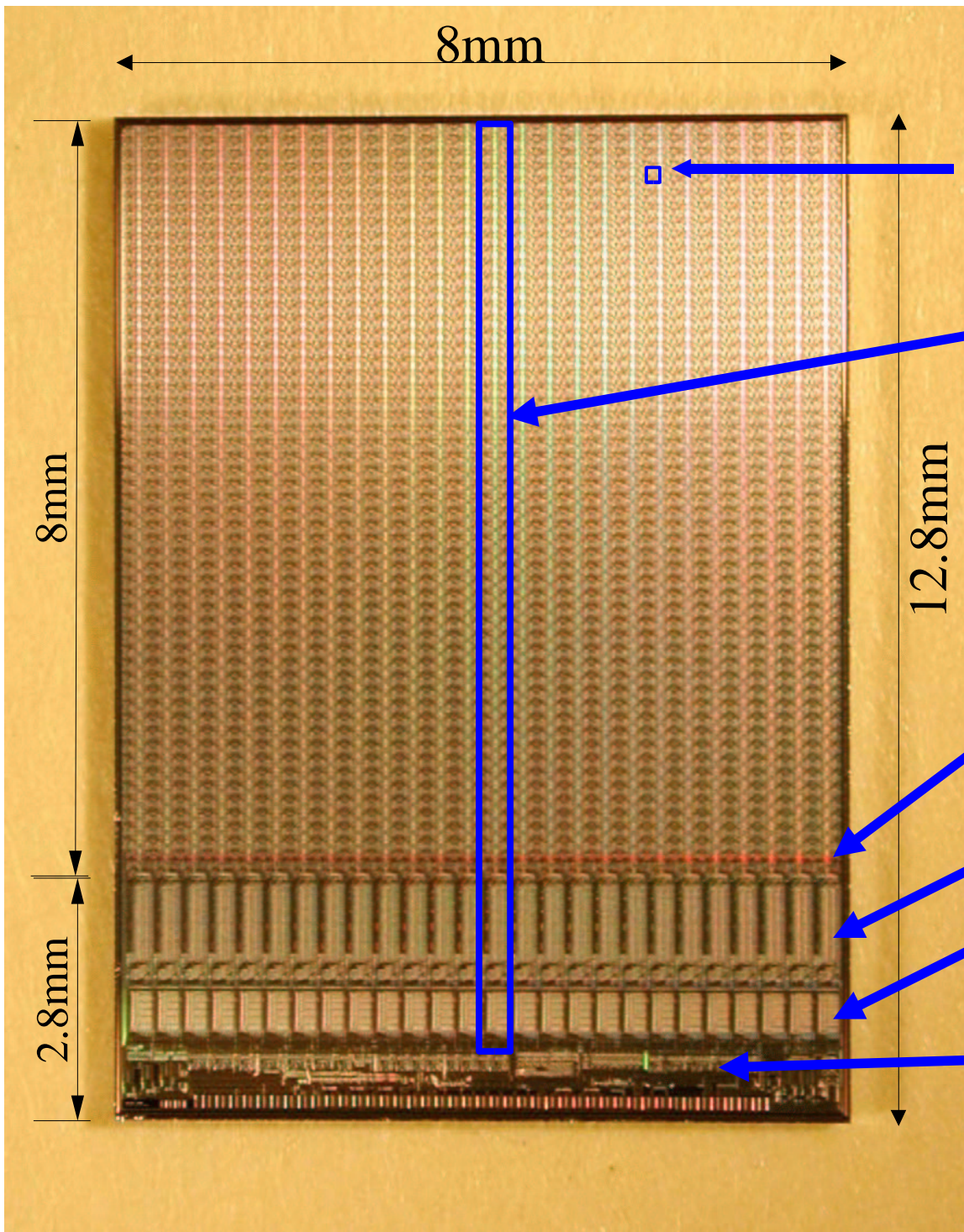


The DMILL readout chip of the CMS pixel detector

Wolfram Erdmann
ETH Zürich
Pixel 2002
Carmel, September 2002

- PSI43
- Testbeam



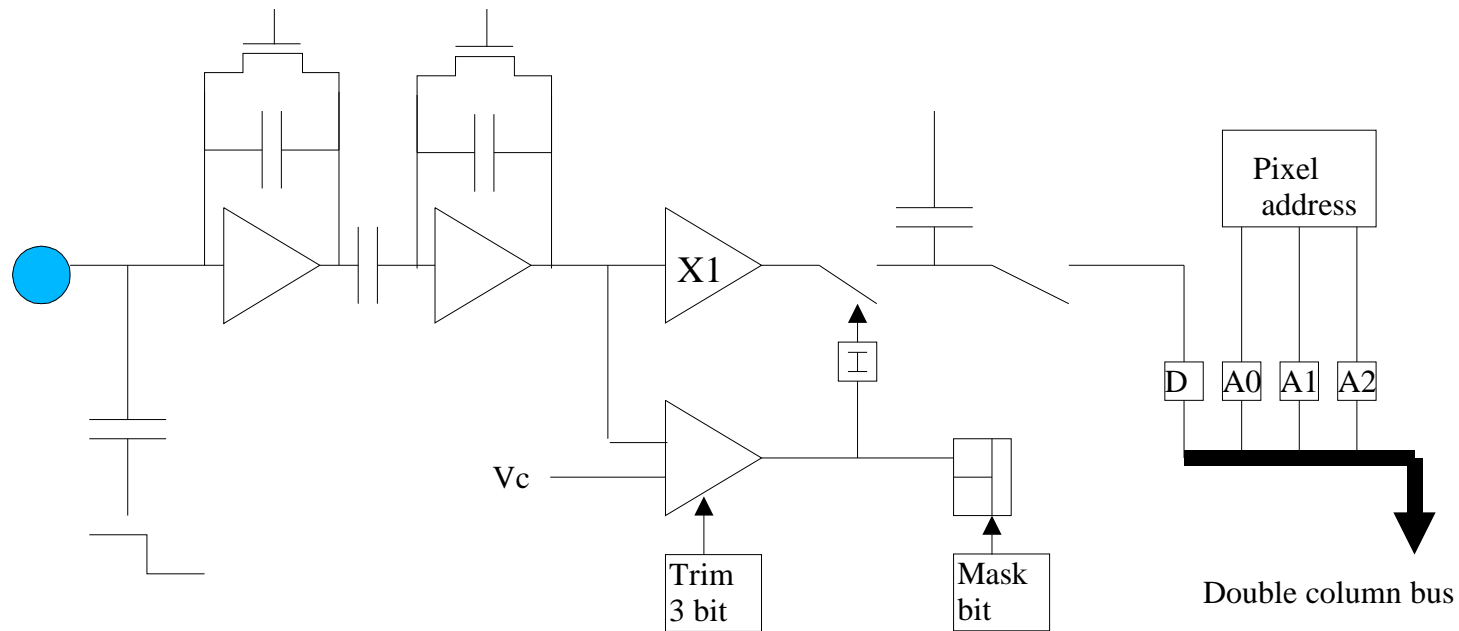
PSI43

- 150 μm x 150 μm pixel
- 52x53 pixels in
26 double columns
345 k transistors
- Periphery:
78 k transistors
- Pixel–column interface
- Data buffers (4x24 capacitors)
- Timestamp buffers (8x8 bits)
- I2C, DACs, regulators,
counters, readout, wirebonds
6 k transistors

PSI43, CMS pixel readout

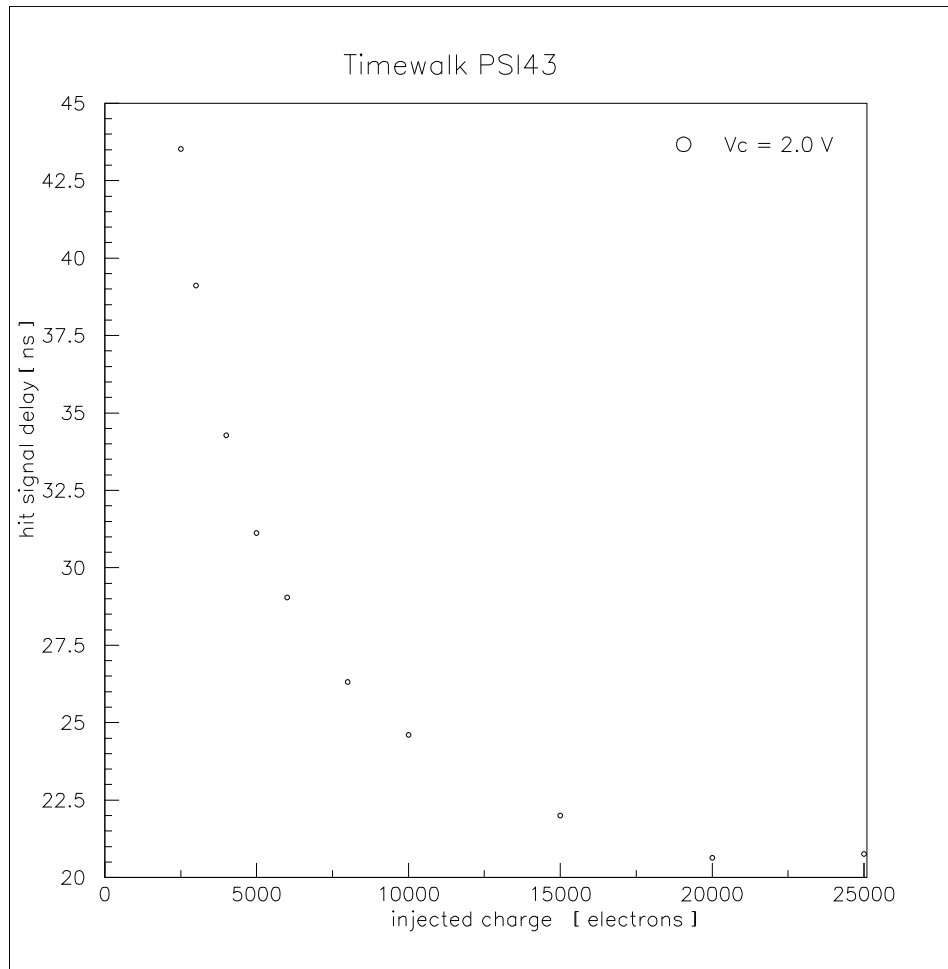
- CMS/LHC:
 - 40 MHz bunch crossing frequency
 - up to $25 \cdot 10^6$ tracks/cm²/s
 - 40 kHz trigger/readout, small dead-time
 - Analog pulse-height information for cluster reconstruction
- Radiation hard DMILL process
 - 0.8 μ m CMOS+BJT
 - SOI, 2 metal layers
 - => design: limited # of transistors/pixel, bus lines

Pixel Front-End



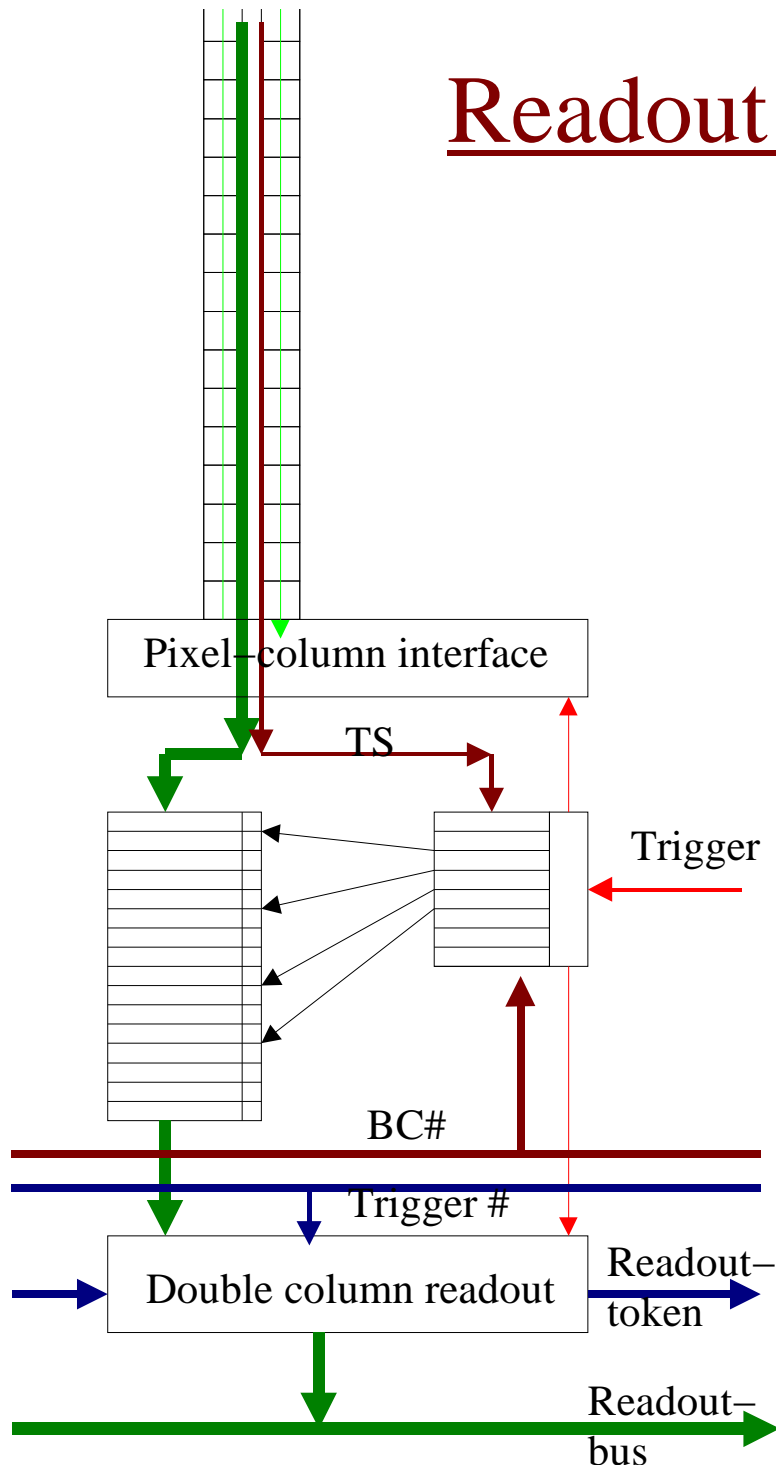
- Preamplifier/Shaper, comparator, sample&hold
- Comparator threshold adjustable: global V_c (8bit) + Trim-scale (8bit) + local trim (3bit)
- 1.6fF calibration capacitance, enabled row/column-wise
- Pixel addresses: scaled current sources

Front-End



- preamp/shaper: 40uW/pixel
- Time-walk < 25ns
(comparator output)
for >2500 e signal charge
- Intrinsic noise 120 e
- 10nA leakage current
tolerable

Readout Architecture



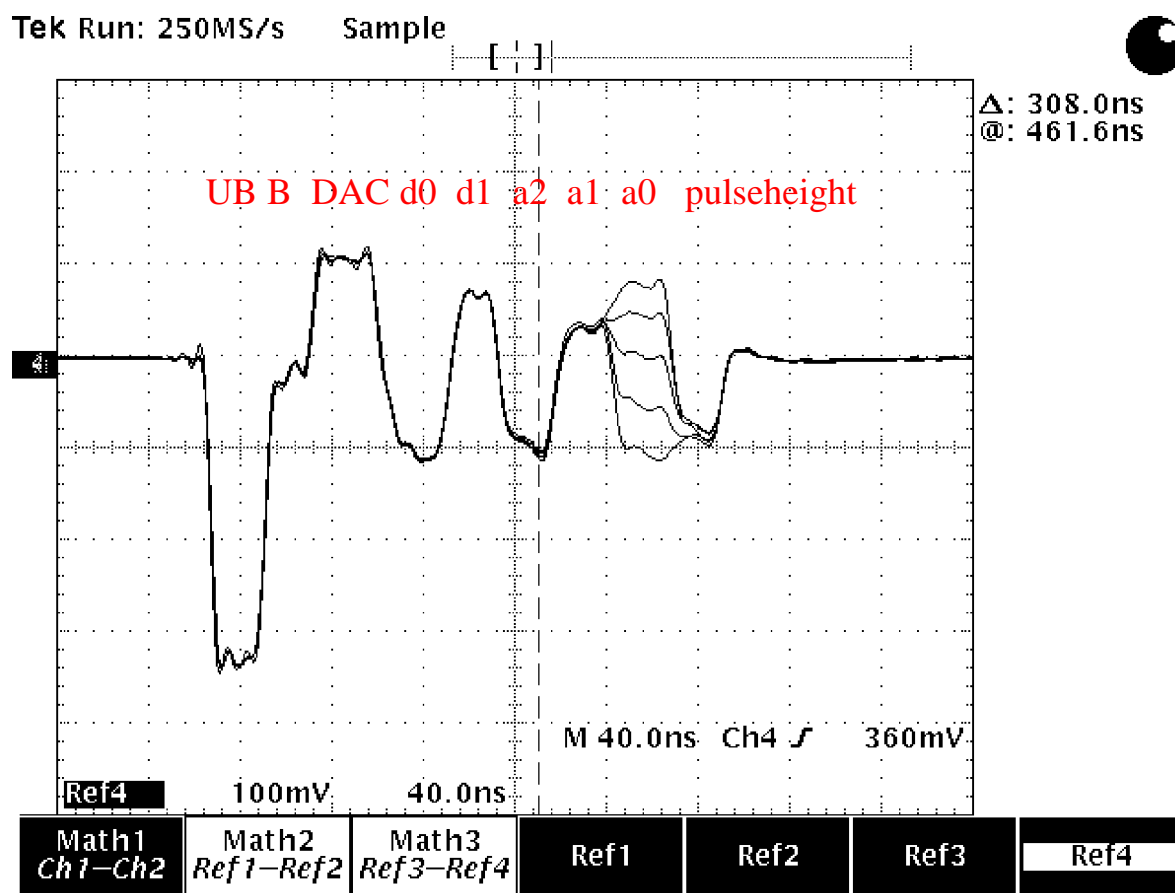
- Organized in double columns
- Column Drain: hit pixels move data to buffers in the periphery as fast as possible
 - 1) store bunch crossing in time-stamp buffer
 - 2) create marker in data buffer and copy data + address (20MHz)
- Data are kept during trigger latency
- A matching trigger stops the double column, latches trigger #
=> waits for corresponding readout-token

PSI43 Control&Interface

- Chip Configuration with serial bus ($\sim I^2C$)
 - Pixel trimming/masking/calibration
 - 21 DACs
 - Trigger Latency, readout mode
 - Chip address by wire–bonding, no direct readback
- Data acquisition controlled by 3 digital signals (differential LVDS)
 - 40 MHz bunch crossing clock
 - Trigger, also used for calibration and (soft)reset
 - Readout token, for daisy chained readout

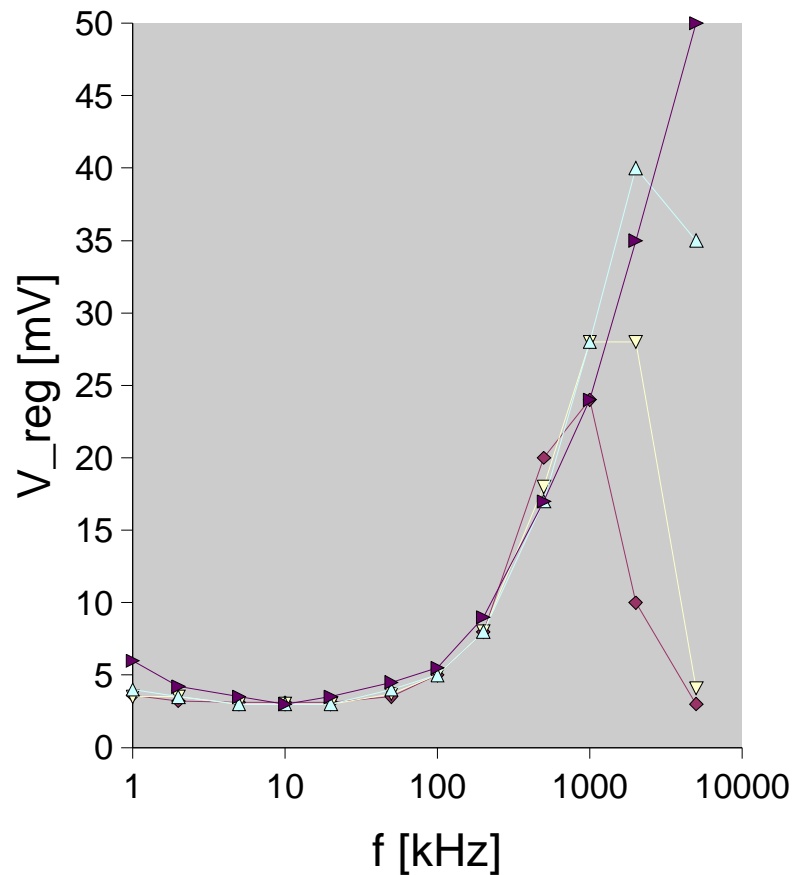
Analog Readout

- Daisy chained readout (token passing)
- 3 cycle chip header
 - UB,B → chip ID
 - DAC → only status output
- 6 cycles pixel data
 - Analog coded address, 5 levels
 - Pulseheight
 - Repeated for each pixel
- 20MHz/40MHz readout speed selectable (I2C)



Regulators

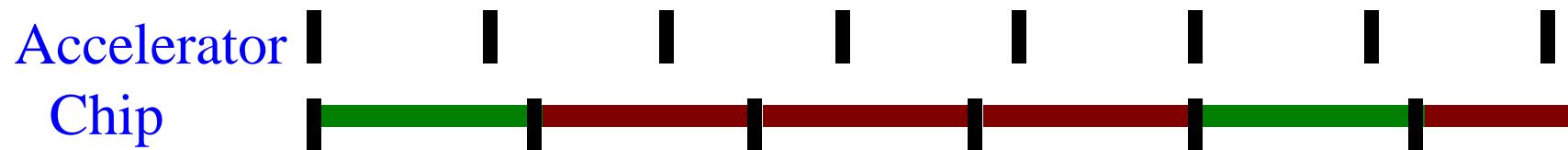
PSI43 regulators



- On-chip regulators
 - Compensate voltage drops on different length cables/varying current
 - Improve PSRR for analog parts
- Effective up to 200 kHz
- Bond pads available for additional caps
- Curves 0–82 nF
5V±100mV input, 0.5V dropout, 30mA

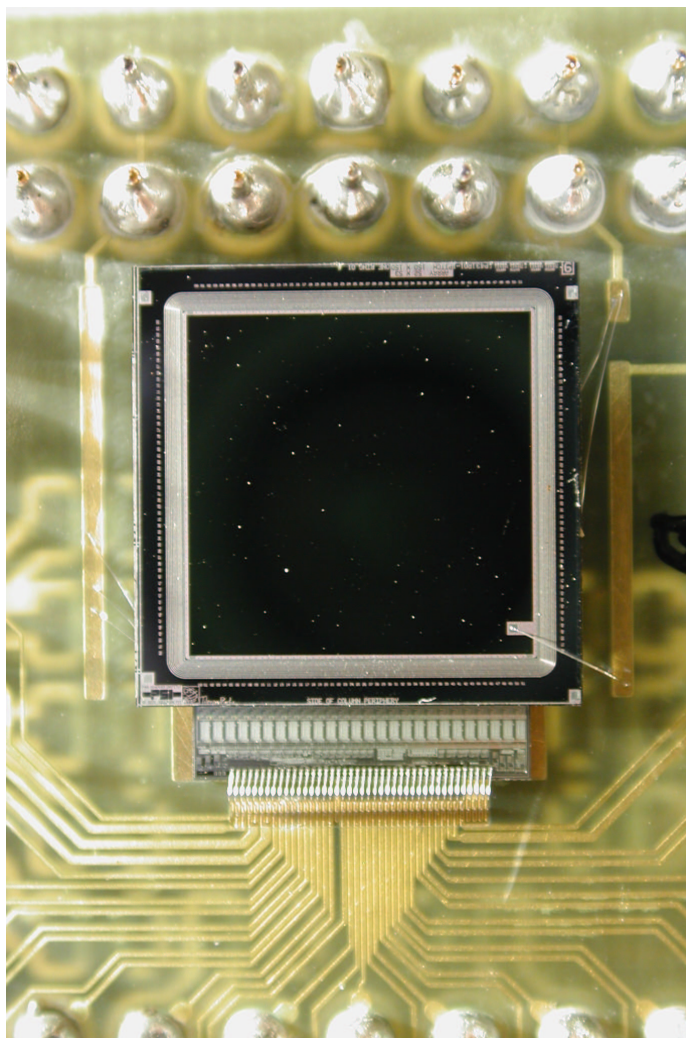
Testbeam, PSI July/August 2002

- 350 MeV/c, mostly π^+ , 50 MHz beam structure
chip operated with synchronized 40 MHz clock



- Intensity variable, up to $30 \times 10^6 / (\text{cm}^2 \text{s})$
track density \approx high Luminosity, 4 cm radius
- Beam-spot 10mm x 20mm (FWHM) \rightarrow covers one chip
- **Test of the chip/readout architecture**
 - Rates comparable to LHC conditions
Stochastic hit patterns

PSI testbeam

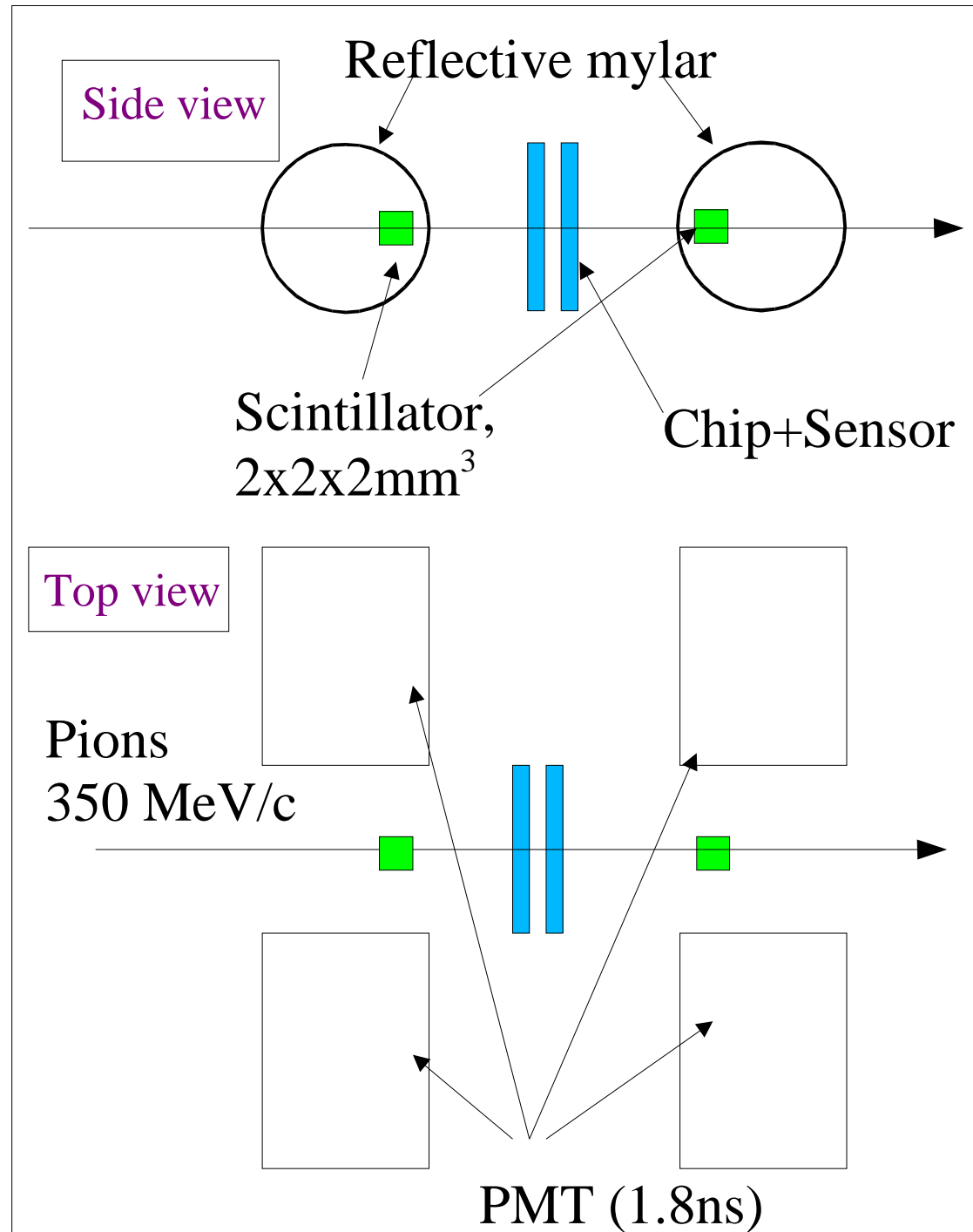


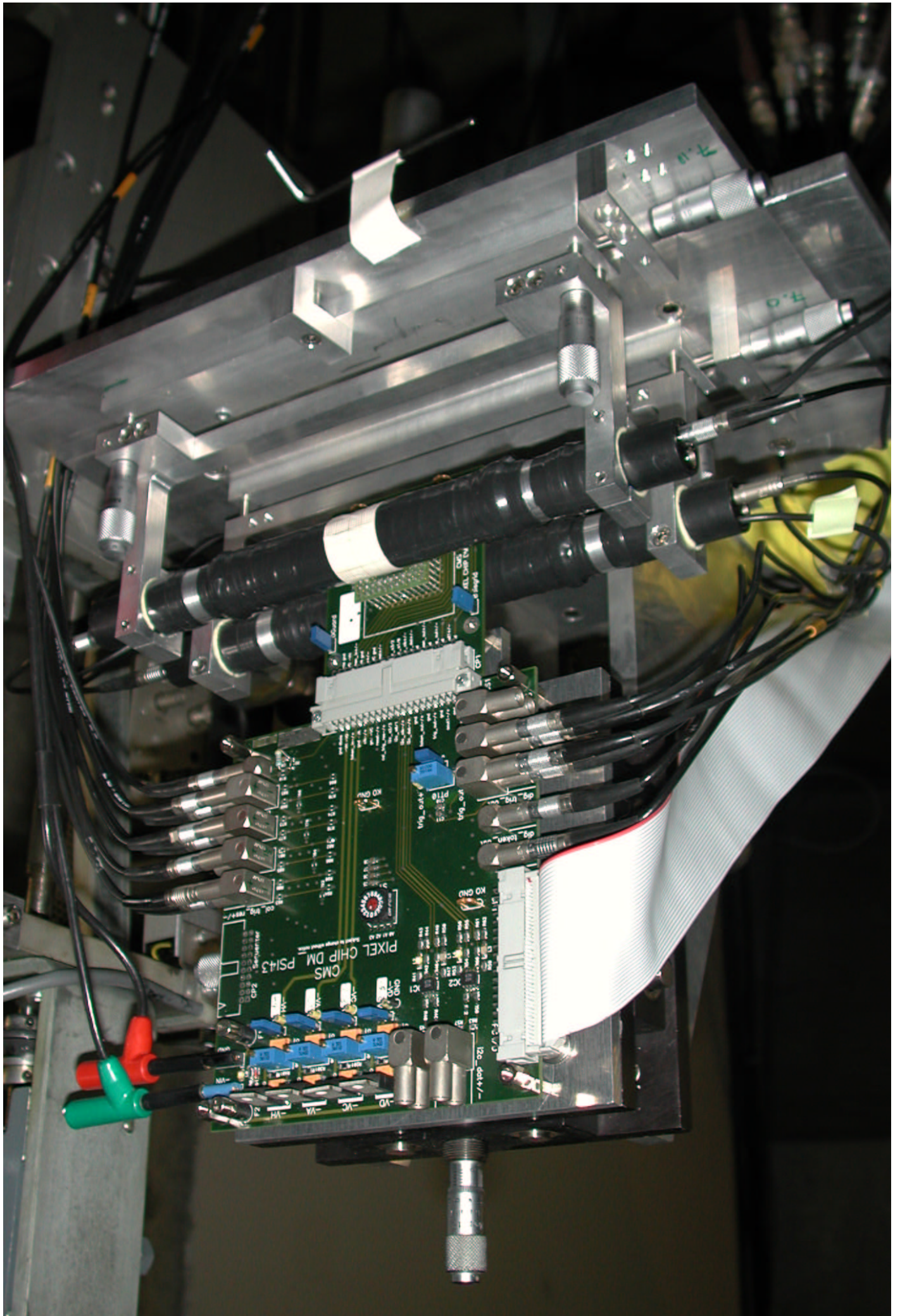
- Bump-bonded single chip + sensor assembly
- Control
 - I2C → PC
 - Clock, Trigger, Readout Token → NIM + FPGA
- Readout
 - VME ADC

PSI testbeam setup

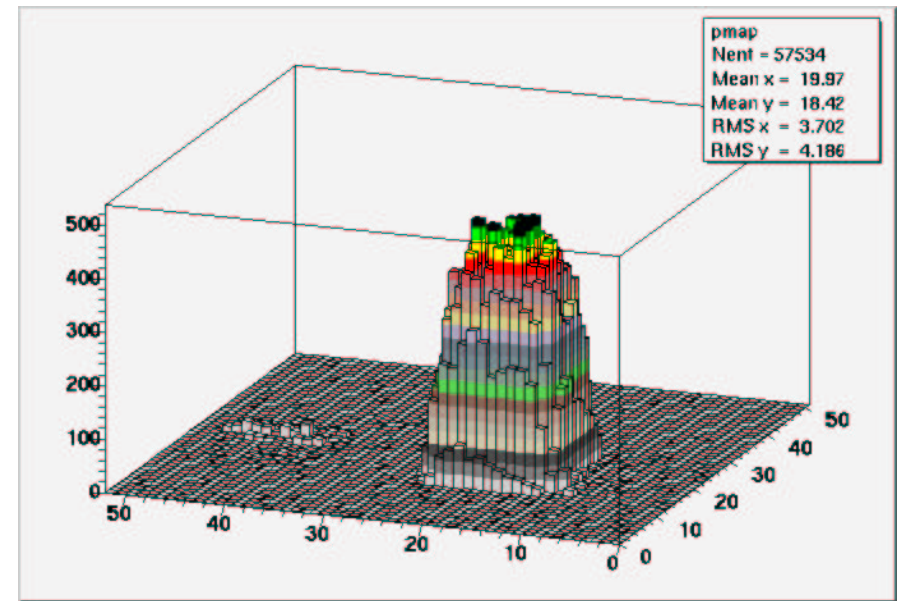
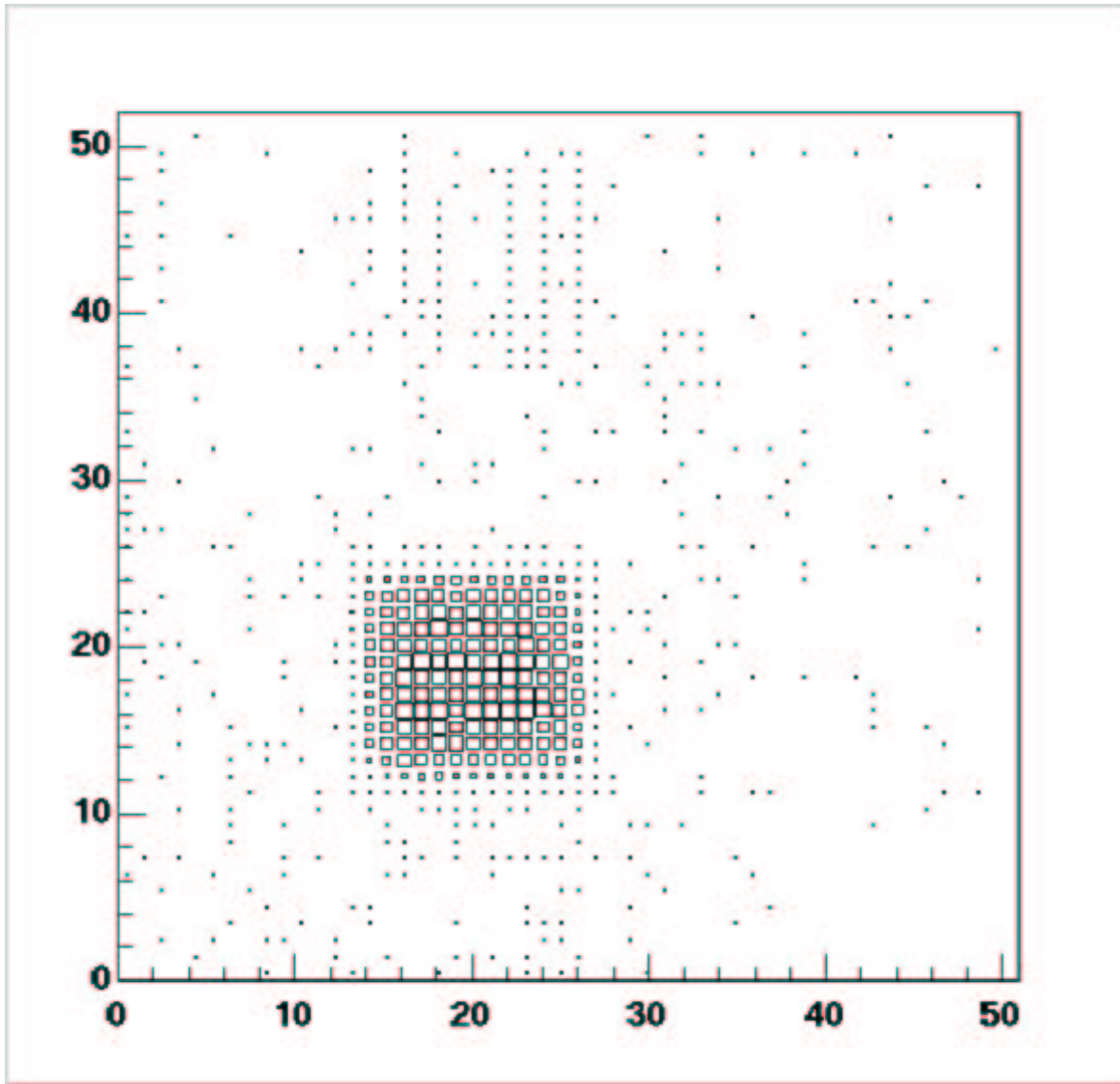
Scintillators

- Monitor beam intensity
- Trigger on beam particles
→ efficiency/data-loss
very clean trigger
needed
- Adjust trigger rate by
coincidence w/random
triggers (source)



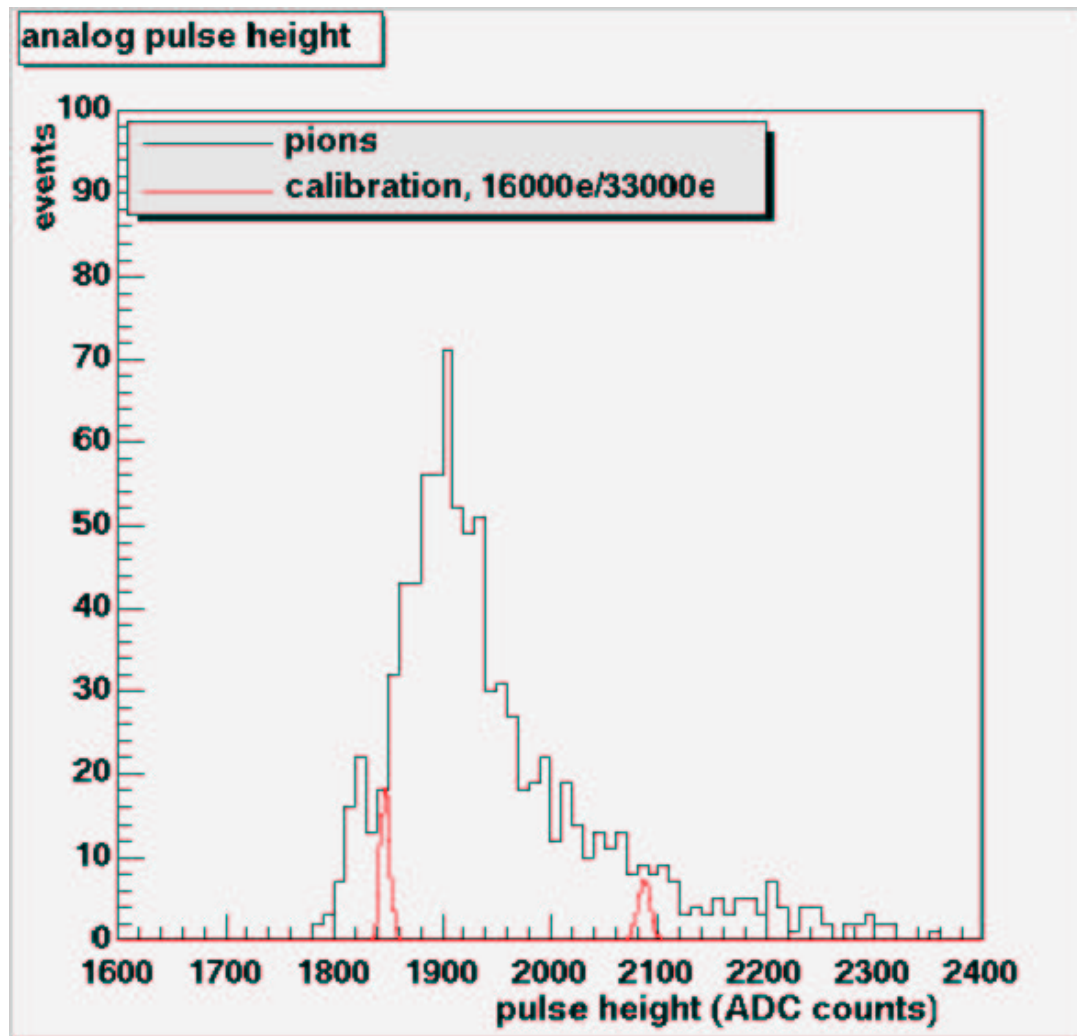


Address readout



- Analog address encoding
- Large level variations among double columns
- Reconstruction still possible
- Small fraction of misidentified row addresses at 40MHz

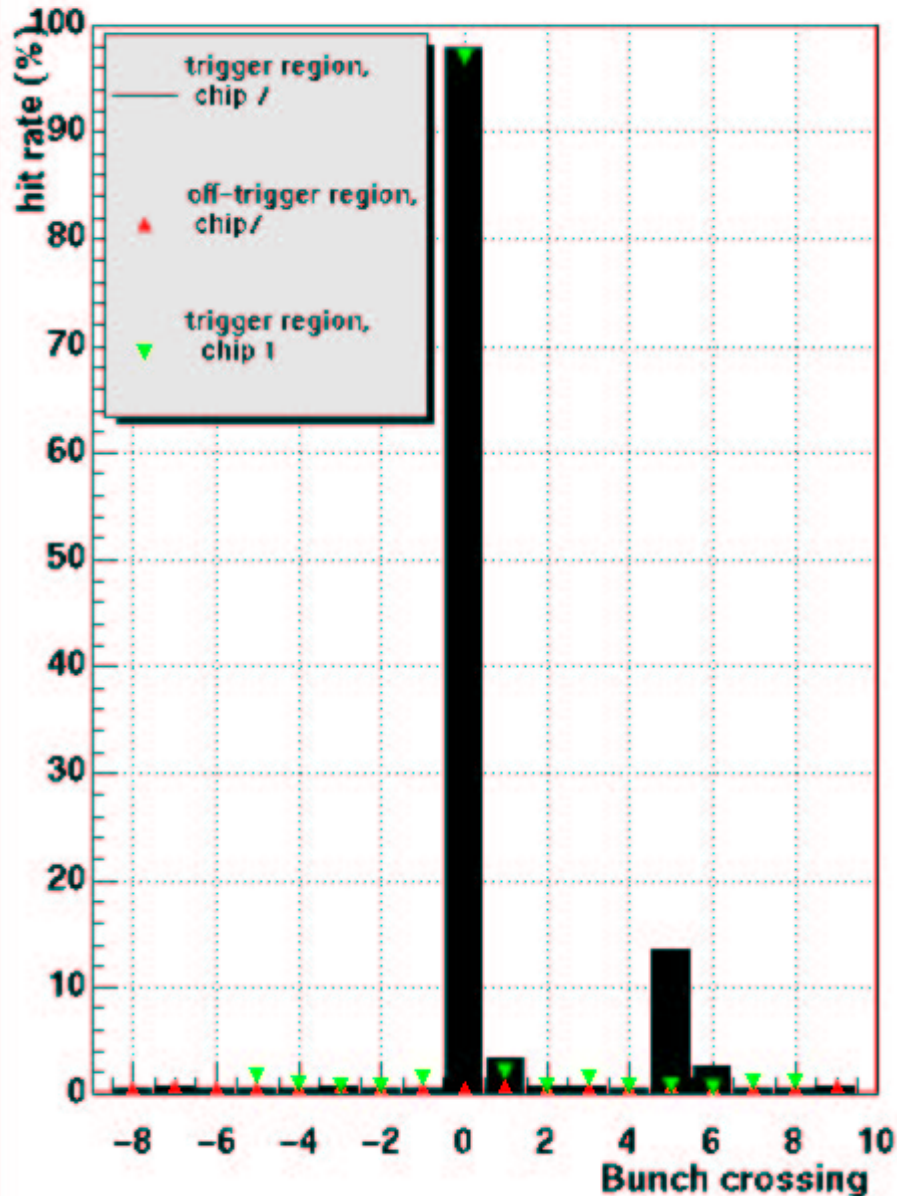
Pulseheight readout



- Pulseheight distribution, single pixel
- 280 μm sensor, 350 MeV/c pions (MIPS)

Timing

- Pions, triggered with scinitillator time spread 4.6 ns (2σ)
- 98% of the hits get the correct time-stamp
- ~2% spill-over into next bunch crossing
- Additional entries at (n+5) BC observed in one of two chips
- Periodic structure of random hits due to 40/50 Mhz



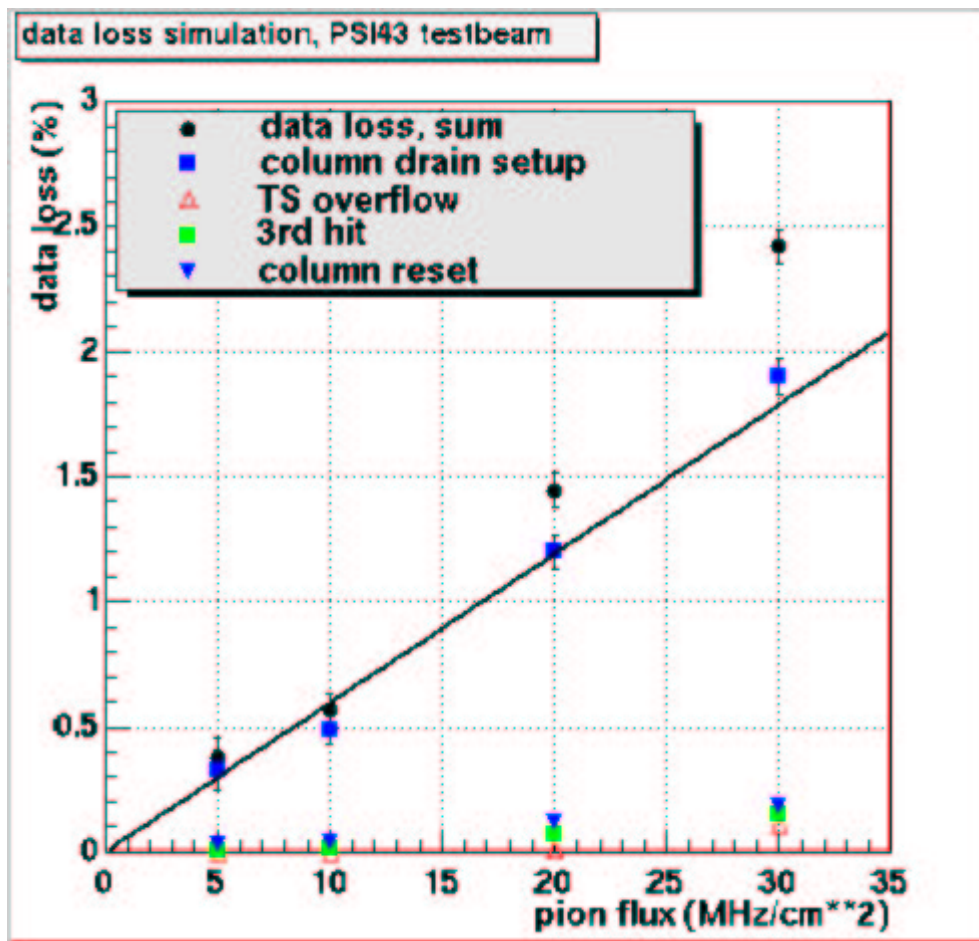
Data–loss

- Architecture not completely deadtime–less
- Fluctuations in the data rate lead to data loss
- Simulation of high luminosity CMS conditions:

Layer	7cm	4cm	
Luminosity	10^{34}	10^{34}	Reason
CD setup	1.80%	3.90%	Hits in two consecutive bunch crossings
Column busy	0.23%	0.95%	>1 new TS during column scan
Pixel overwrite	0.16%	0.38%	New hit in pixel while waiting for column drain
DB overflow	0.04%	0.12%	>24 hits during trigger latency
TS overflow	0.05%	2.80%	> 8 time stamps during trigger latency
Double column reset	0.21%	0.59%	New trigger btw prev trigger and readout
Total	2.70%	9.00%	

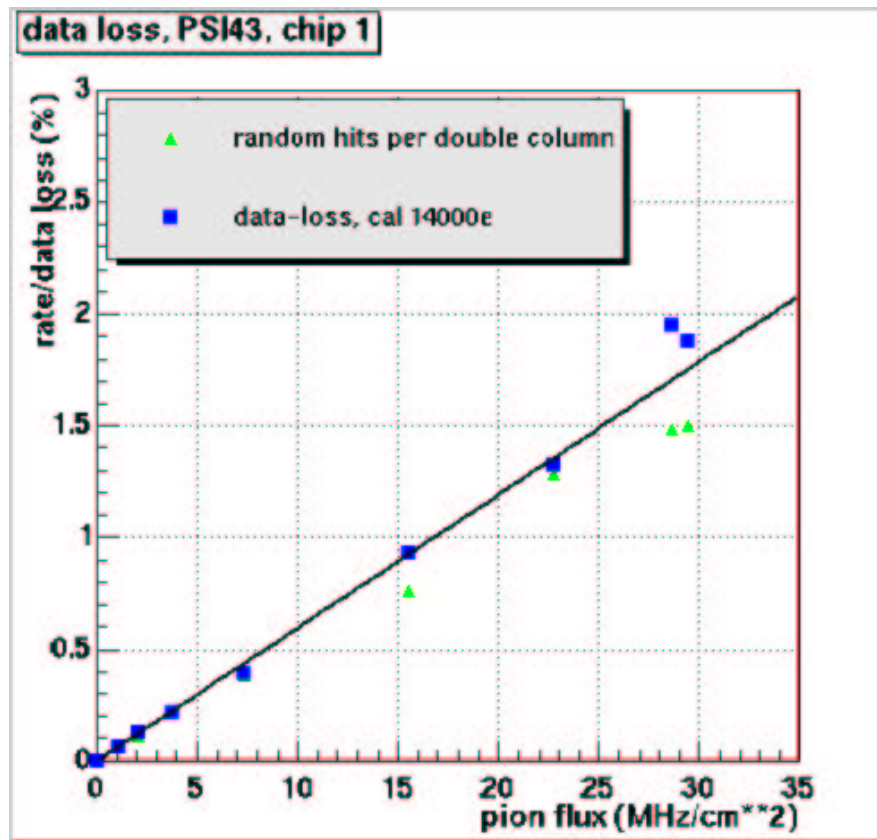
- <1% at low luminosity

Testbeam data–loss simulation



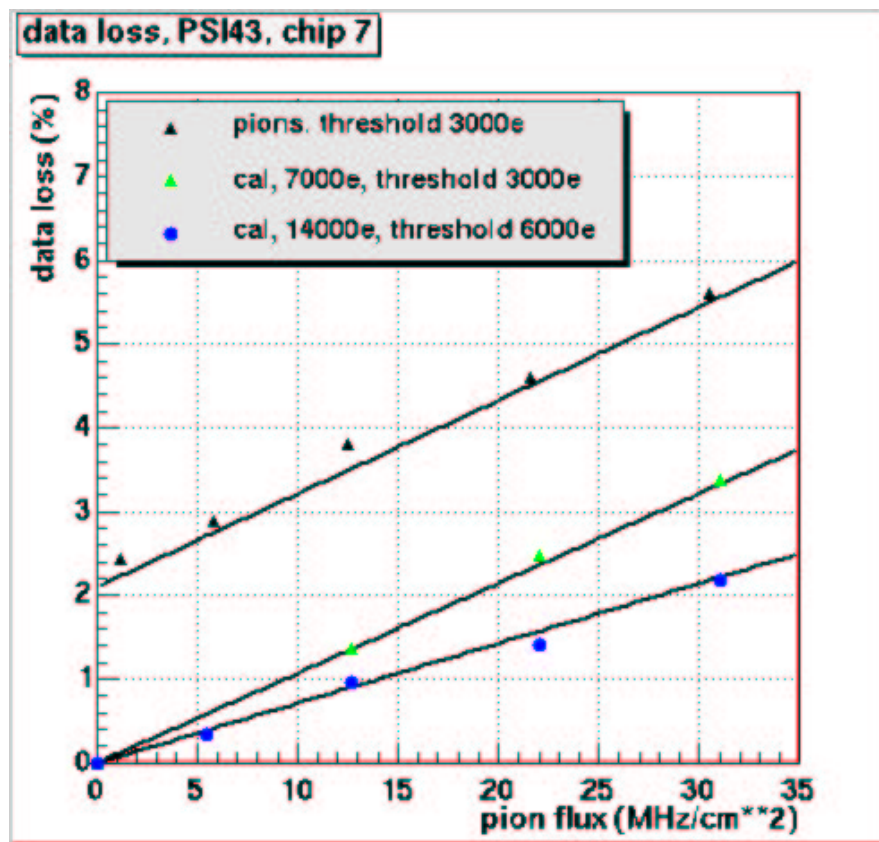
- Particle flux comparable to LHC, but lower pixel multiplicity
 - perpendicular tracks
 - no B–field
- Deadtime due to hits in consecutive bunch crossing (same double column) expected to dominate

Testbeam data–loss measurement, artificial "hits"



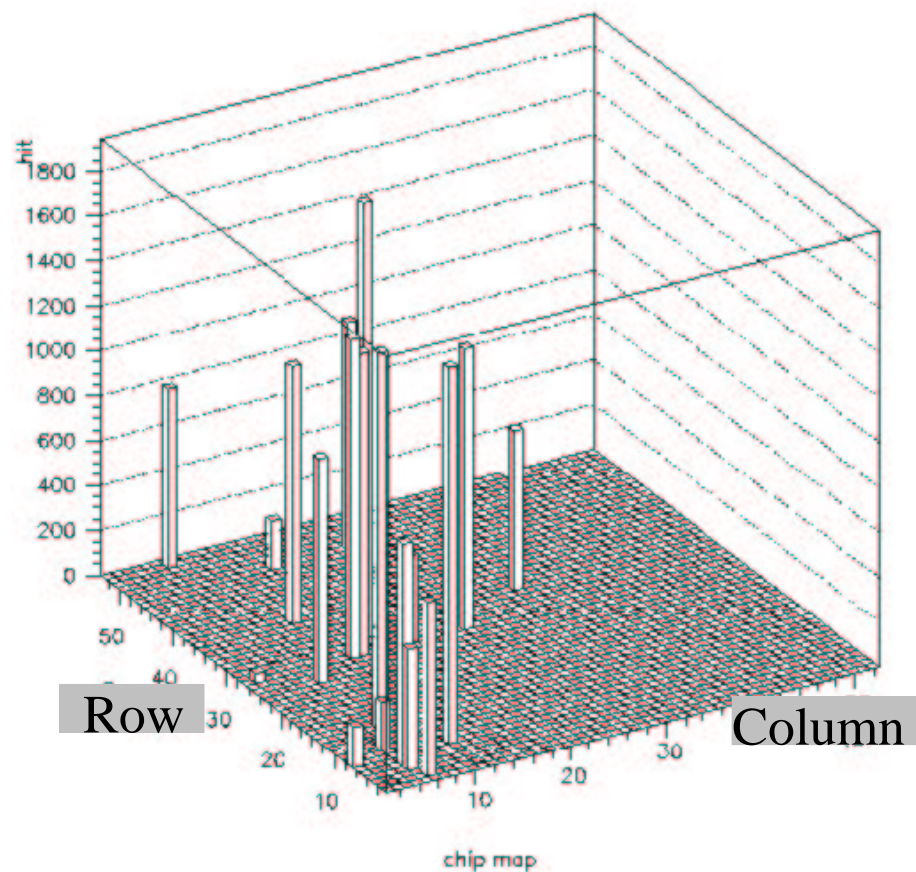
- Inject calibration signals on top of the beam induced hits
- Send trigger/token and count missing hits
- 100% efficient without beam induced traffic
- Linear increase with beam intensity
- Data loss \sim random hit rate per double column

efficiency for beam particles



- events triggered with scintillators
- 2% inefficiency for very low beam intensity
- Steeper increase with beam intensity than expected
- Similar slope observable for calibration signals at low threshold

Single Event Upset



- Look for SEU in Mask bit FF (minimal transistors, 4.5V, 2756 FF/chip)
- Start with all pixels masked
- 17 pixels (0.6%) responded after 6½ h pion irradiation, 18 MHz/cm²
- $\Rightarrow \sigma = (1.5 \pm 0.4) \cdot 10^{-14} \text{ cm}^2$
- Compatible with earlier results, higher rate expected for trim bits

Summary

- PSI43, first full readout chip for the CMS pixel detector in DMILL technology
- Basically working, room for improvements
- Successfully detected particles in a high rate pion beam at PSI
- Readout architecture works adequately
- Slightly higher inefficiency than expected at high flux/low threshold